SEE Tests for Texas Instruments ADS5424 ADC

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Test Date: 11/12 to 11/15/07; and 6/18/08 to 6/23/08

I. Introduction

This study was being undertaken to determine the Single Event Upset (SEU), Multiple Bit Upset (MBU) and Single Event Latch-up (SEL) susceptibility of Texas Instrument ADC converter: ADS5424. Tests were performed with heavy ions at the Texas A&M Cyclotron Facility.

II. Devices Tested

There are a total of 3 ADC being tested. 2 will be made available for this test suite, including 1 control sample. Due to time constraints, we were not able to build a specialized DUT board. We are therefore using a Texas Instrument Evaluation board with one embedded ADC (DUT). The Evaluation board number is ADS5411EVM. The identification information for these ADCs is as follows:

Test Chip: ADS5424

Lot #5962

Full Part Number: 5962 0720601VXC ADS5424MHFG-Y THA 7BAR 0725A

The device technology is Texas Instruments complementary bipolar process BiCom3x. The following are some of the ADS5424 Features (please refer to the ADS5424 datasheet for a complete description):

- 14 bit resolution
- 105 MsPS Maximum Sample Rate
- 2.2 Vpp Differential Input Range
- 5v Power supply
- 3.3V compatible outputs
- 1.9W total power Dissipation
- 2s complement output
- 52 pin package
- Industrial temperature range of –40C to 85C

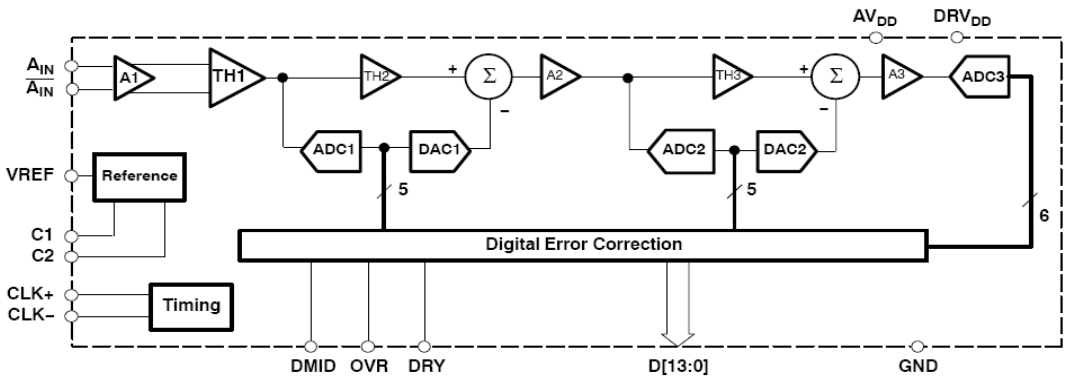

Figure 1: Functional Block Diagram of the ADS5424

Table 1: Evaluation Board Pin Out

J9 PIN	DESCRIPTION	J9 PIN	DESCRIPTION
1	CLK	21	DATA BIT 6
2	GND	22	GND
3	NC	23	DATA BIT 7
4	GND	24	GND
5	NC	25	DATA BIT 8
6	GND	26	GND
7	NC	27	DATA BIT 9
8	GND	28	GND
9	DATA BIT 0 (LSB)	29	DATA BIT 10
10	GND	30	GND
11	DATA BIT 1	31	DATA BIT 11
12	GND	32	GND
13	DATA BIT 2	33	DATA BIT 12
14	GND	34	GND
15	DATA BIT 3	35	DATA BIT 13 (MSB)
16	GND	36	GND
17	DATA BIT 4	37	OVERFLOW
18	GND	38	GND
19	DATA BIT 5	39	DRV_{DD}
20	GND	40	GND

Table 2-2. Test Point Description

TEST POINT	FUNCTION
J14	Monitor Vref (AVDD/2)
J17	Monitor DMID (DVDD/2)

III. Test Facility

Facility: Texas A&M Cyclotron Facility

Flux: ~10^3 ions/cm^2/s

Fluence: SEU/MBU tests will be run until (1) sufficient statistics are obtained 10^6 - 10^7 ions/cm^2 (2) an increase in supply current (I_{dd}) is seen (3) or a SEFI is observed;
SEL tests will be run until (1) an increase in supply current is observed, (2) or a fluence of 10^7 ions/cm^2 is reached.

IV.
V. Test Conditions and Error Modes (Test Methodology Overview)

Test Temperature: Room Temperature for SEU/SET; up to 85°C for SEL

Operating Frequency: 1MHz, 50MHz, and 100MHz ADC clock and ADC data input (during initial testing both input frequencies are always equal.

Power Supply Voltage: V_{dd} = 5V ; I/O = 3.3 V; Stress tests at 5.25V and 4.75V

Data Inputs: Supply Sine Waves from functional generator (as ADC data input) at varying frequencies (1MHz, 50HMz, 100MHz). Supply ADC clock signal at varying frequencies. (See section VI.B)

Angular Data: Data was only taken at 0 degrees (incident angle), due to the size constraints of the TI evaluation board.

Recovery from SEL: In the case of potential SEL observation, the test-setup must be able to determine if recovery is possible without power cycling. If recovery does not occur, power supply voltage should be incrementally lowered to determine the point at which recovery is observed. SEL classification will be determined by observing a sharp current jump on the LabView monitor. Current stays at high level.

Monitoring TID: Supply (leakage) current (I_{dd}) was measured after each irradiation to monitor parametric degradation from TID.

Data Input Error Mode:

1) All upsets must be time tagged containing erroneous value and expected value.
2) A calculation of the average value (1024 samples pre-irradiation) will be used as the golden compare. The golden/expected value will be updated (1024 values that are not considered in error) every 8 ms in order to protect against drift.
3) Data range settings will be set by user and are utilized in the data comparison

$$val\_low \le Datainput \le val\_high$$
$$val\_low = ExpectedValue - error\_range$$
$$val\_high = ExpectedValue + error\_range$$

SEE Conditions: SEFI, DUT board current level shifts, and bad data points.

Sections V and VI below are TBD. ***See Appendix 1 for design information from TI.***

VI. Test Methods

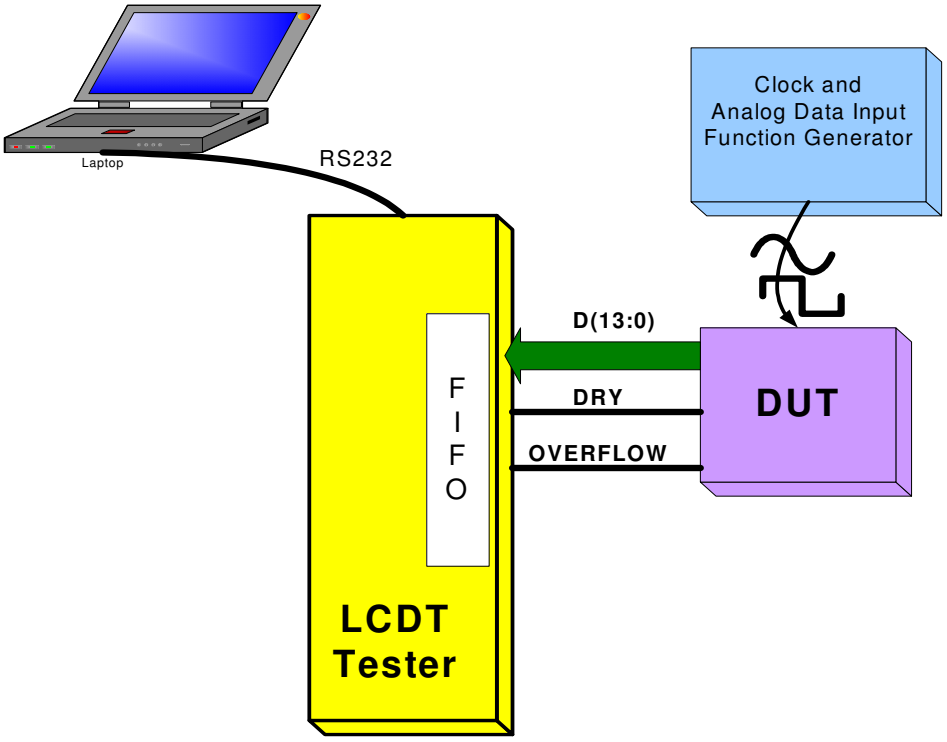

Figure 2: Tester to LCDT Topology

A. Test Set-up

Figure 2: Tester to LCDT Topology illustrates the test set-up. There will be a user pc to supply the commands (such as start test, reset, and other test parameters (i.e. frequency control). There will be one frequency generator that will supply the square wave clock input to the ADC and one that will supply the sine wave data input to the ADC. The tester will be used purely to gather data from the evaluation board. Data shall be collected at every rising edge of DRY. Each data item will be compared to an expected value. If there is an error (mismatch), then the data item is time stamped and sent (with its associated expected value) to the user PC via the RS232.

B. Tests

There will be several types of tests performed by varying a) frequency of data input and b) frequency of clock.

1. Clock=100MHz and Data Input = 100MHz. Expected is calculated pre-irradiation (per test). Amplitude shall vary: 0db and10db
2. Clock=50MHz and Data Input = 50MHz. Expected is calculated pre-irradiation (per test). Amplitude shall vary: 0db and10db
3. Clock=1MHz and Data Input = 1MHz. Expected is calculated pre-irradiation (per test). Amplitude shall vary: 0db and10db

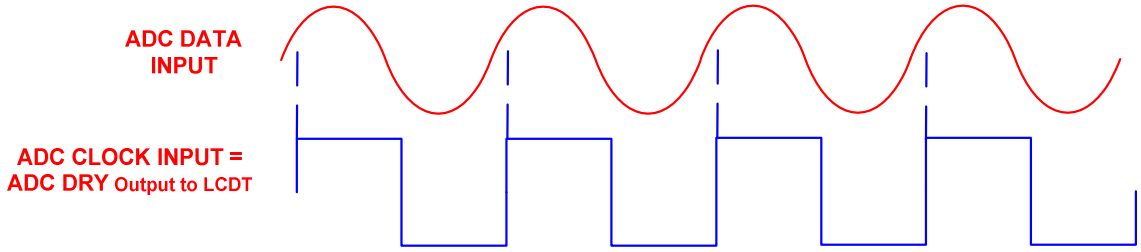

Figure 3: Tests 1 thru 3 only have one sampling point per sin period

4. Clock = 100MHz and Data Input = 25 MHz. There will be 4 expected values Amplitude shall vary (we will try to find worse case)
5. Clock = 100MHz and Data Input = 12.5 MHz. There will be 8 expected values Amplitude shall vary (we will try to find worse case)

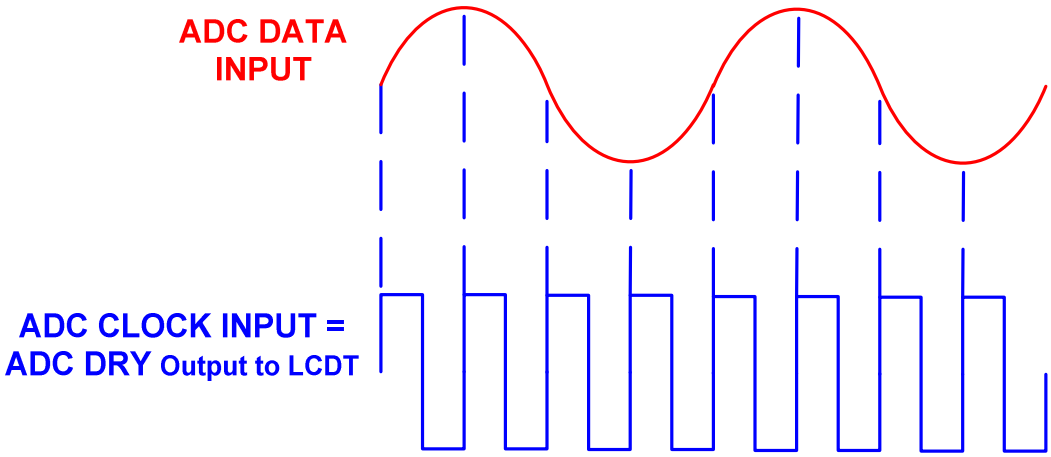

Figure 4: Tests 4 and 5. Clock is faster than data input - provides more test points

6. Potential test: Data input = 100MHz and Clock input = 99MHz.

** Tests 2 - 4 may be performed in February 2008

C. Test Commands

The User controls the tests via a LABVIEW interface running on a PC. The PC communicates with the LCDT with a RS232 serial link. The format of communication is a command/Data 4 byte word.

Table 2 : Summary of Commands Used in Eclipse Tester

Command #HEX	Command	D0	D1	D2	Description
01	Reset DUT	N	N	N	Resets Tester
02	Start Test	N	N	N	Starts gathering ADC data
B0	Error Range	Y	N	N	(exp value-Error_range) < ADCout < (exp value+Error_range);[0 … 255]; default=0
A0	Clock Frequency	Y	N	N	Clock frequency divider of 100mhz; [2...255] default = 1

The following is a detailed description of commands and their associated functionality.

1. RESET DUT:

The RESET DUT command is decoded as x01. The following represents the command as noted in Table 2:

x01	xx	xx	xx

Figure 5: Reset Command Format – Command Number, D0, D1, and D2

Once decoded, all DUT inputs will go into reset mode (Reset, CLK_SR and D_SR are low)

2. START TEST:

START TEST is decoded as x02. The following represents the command as noted in Table 2:

x02	xx	xx	xx

Figure 6: Start Command Format

All other commands should be supplied before start test. I.e. the user should define the pattern and clock frequency before administering a start. This command activates the CLK_SR and D_SR DUT inputs.

3. Error Rage:

Error Range is decoded as xB0. The following represents the command as noted in Table 2:

xB0	xnn	xx	xx

Figure 7: Start Command Format

This command must be supplied before the start test (unless using the default value= 0).

4. CLOCK FREQUECY:

The clock frequency command is decoded as xA0 utilizing byte D0. The following represents the command as noted in Figure 8:

xA0	xnn	xx	xx

Figure 8: Clock Frequency Command Format

Upon the receipt of this command, D0 is used as a clock frequency divider. This command must be sent after a RESET DUT and before a START TEST. D0 must be an even number and must be greater than or equal to 2. The associated output is CLOCK_FREQ. See the LCDT General Tester for more information concerning the processing of CLOCK_FREQ.

D. Running a Test

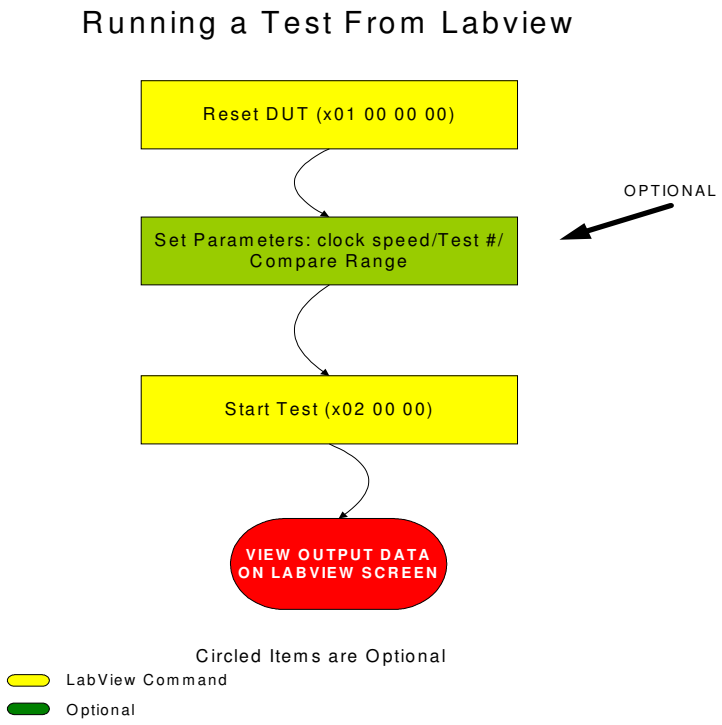

Figure 9: Flow Diagram of Running an ADS5424 Radiation Test

VII. Test Results

All tests in Table 3 were performed at room temperature and were monitored for SEU/MBU including SEL. Flux was set ($1e^4$ ..$1e^3$). The fluence stoppage criteria was 1e6.

Tests (see section VI.B) were run with the LETs and voltages listed in Table 3 and Table 4.

Table 3: SEE Tests. Tests 1 through 4 Shall be Run for each Table Item

ION	Angle	LET (MEV/cm2/mg) 0 deg	Voltage
Ar	0	8.5	5V
Kr	0	28.5	5V
Xe	0	52.7	5V

All tests in table 4 will be run with the worse case test (determined in above tests). The Test at Xe 5.25V & 85C will be used to stress SEL conditions.

Table 4:Voltage Variation: Observation of Voltage Effects on SEE and SEL

ION	Angle	LET (MEV/cm2/mg) 0 deg	Voltage	Temperature
Ar	0	8.5	5.25V	Room Temp
Xe	0	52.7	5.25V	Room Temp and 85C
Ar	0	8.5	4.75V	Room Temp
Xe	0	52.7	4.75V	Room Temp

No destructive single events were observed during this test. SEEs occurred at all tested LETs. The figure below is a heavy ion graph of observed error cross-section vs. LET.

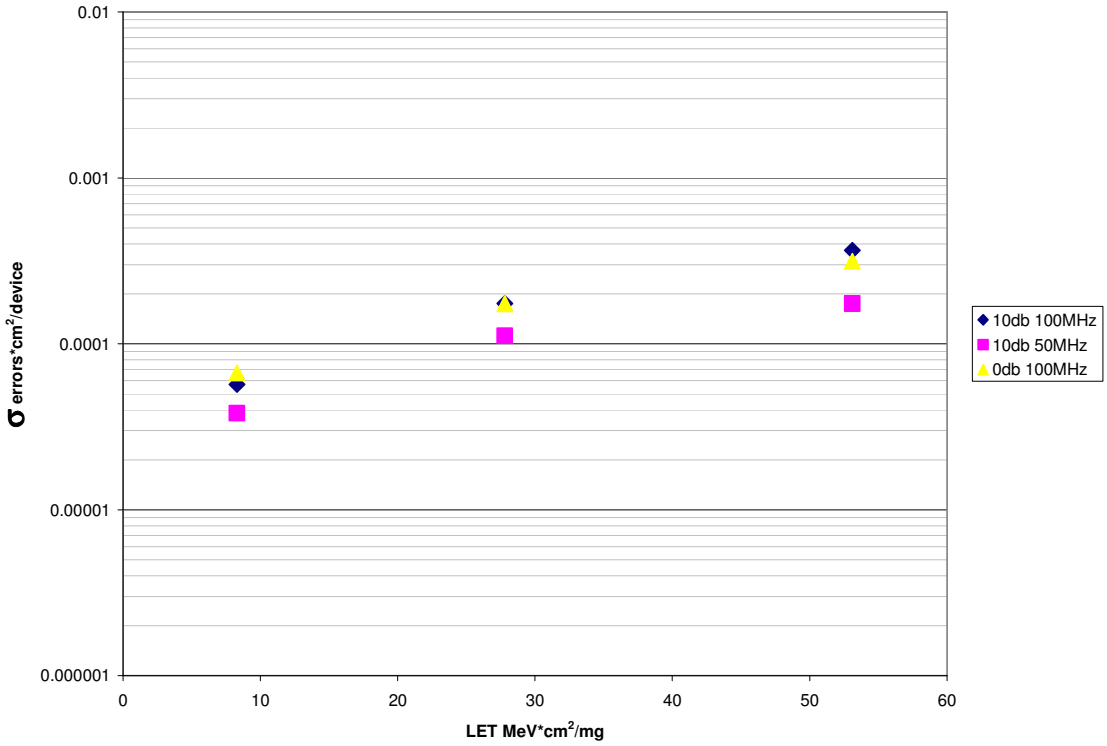

Figure 10:TI ADC5424 Error Cross-Section vs.LET

VIII. Appendix

Applicable documents can be found at:
http://focus.ti.com/docs/prod/folders/print/ads5424.html